AFOSR-TR- 91 0050

(2)

DEVELOPMENT OF Si/SiGe HETEROSTRUCTURES

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January 1991

Final Report
September 1987 through August 1990

Sponsored by
Defense Advanced Research Projects Agency
DARPA Order No. 6140/00
Monitored by AFOSR Under Contract No. F49620-87-C-0104

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SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION / AVAILABILITY OF REPORT Approved for public release; distribution unlimited.
2b. DECLASSIFICATION / DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S)	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION Hughes Research Laboratories 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Directorate of Electronic and Material Sciences AFOSR
6c. ADDRESS (City, State, and ZIP Code) 3011 Malibu Canyon Road Malibu, CA 90265	7b. ADDRESS (City, State, and ZIP Code) Building 410 Bolling AFB, DC 20332-6448
8a. NAME OF FUNDING / SPONSORING ORGANIZATION DARPA 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F49620-87-C-0104
8c. ADDRESS (City, State, and ZIP Code) 1400 Wilson Blvd., Arlington, VA 22209	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. 62712E; PROJECT NO. 6140/00; TASK NO. 00; WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)
DEVELOPMENT OF Si/SiGe HETEROSTRUCTURES

12. PERSONAL AUTHOR(S)
R.J. Hauenstein, J.L. Veteran, M.H. Young

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
Final	FROM 9/87 TO 8/90	1991 January 18	35

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

We have developed new molecular beam epitaxy (MBE) materials growth and doping processes for the fabrication of Si/SiGe heterostructure devices. We applied these new materials processes to the demonstration of cryogenic n-p-n Si/Si_{1-x} Ge_x/Si heterojunction bipolar transistors (HBT). This application has special significance as an enabling DoD technology for fast low noise, high performance readout and signal processing circuits for IR focal plane systems.

We succeeded in developing reliable, versatile methods to grow very high quality Si/SiGe strained layer heterostructures and multilayers. In connection with this program we developed methods to dope the Si and SiGe with B, Sb and Ga. B and Sb were found to be the preferred dopants for p and n regions respectively, of our HBT devices. Our test devices clearly displayed gain enhancement due to the heterojunction and provided useful gains from room temperature down to 10 K.

20. DISTRIBUTION / AVAILABILITY OF ABSTRACT ☐ UNCLASSIFIED / UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS	21. ABSTRACT SECURITY CLASSIFICATION Unclassified
22a. NAME OF RESPONSIBLE INDIVIDUAL Major Gernot Pomrenke	22b. TELEPHONE (Include Area Code) 202-767-4984 22c. OFFICE SYMBOL NE

DD Form 1473, JUN 86 *Previous editions are obsolete*

SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

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SECTION 1

INTRODUCTION AND OVERVIEW

1.1 GOALS OF PROGRAM

The purpose of this program is to develop the technology to utilize $Si/Si_{1-x}Ge_x$ heterostructure materials in novel electronic devices. In particular, we have concentrated our efforts on the $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor (HBT). This device essentially is a dramatically improved version of the familiar Si bipolar transistor. In addition to significant performance advantages made possible through use of the heterojunction, the $Si/Si_{1-x}Ge_x/Si$ HBT is largely compatible with well established conventional device fabrication and processing technologies. As such, the $Si/Si_{1-x}Ge_x/Si$ HBT represents perhaps the most significant near-term leap in Si-based electronics. In fact, during the lifetime of this program, the $Si/Si_{1-x}Ge_x/Si$ HBT has evolved from a theoretically proposed to experimentally proven device concept through the work of several research groups.

The $Si/Si_{1-x}Ge_x/Si$ HBT as developed under this program is very similar to a conventional Si n-p-n bipolar transistor, differing essentially in the use of a $Si_{1-x}Ge_x$ rather than an Si base layer.[1] This modification, and the modifications in base and emitter doping levels that use of the heterojunction makes possible (higher base doping for reduced base sheet resistance and lower emitter doping for reduced emitter-base capacitance), have led to significant and simultaneous improvements in transistor current gain and high frequency behavior over that of conventional Si bipolar transistors. At the same time, the HBT remains compatible with much of the standard Si device processing technologies, the principal exception being extremely high temperature processes such as thermal oxidation, dopant diffusion and implanted dopant activations. However, the general trends in devices toward thinner active layer sizes and smaller lateral dimensions have been driving device processing technologies toward lower peak processing temperatures, and toward minimum time exposure to very high temperatures. This has led to increasing use of techniques such as rapid thermal annealing (RTA). The extension of Si device technology to include $Si/Si_{1-x}Ge_x$ heterostructures is entirely consistent with these trends in processing. Furthermore, because the HBT, unlike other promising $Si/Si_{1-x}Ge_x$ heterostructure devices, essentially is a direct replacement, in terms of both device processing and applications, for the ubiquitous Si bipolar, the $Si/Si_{1-x}Ge_x/Si$ HBT represents the most significant near-term application of heterostructure technology in advancing the practical state of the art of Si based electronics.

1.2 RELEVANCE TO DoD SYSTEMS

The $Si/Si_{1-x}Ge_x/Si$ HBT offers another potential advantage in addition to improved gain and high-frequency operation that makes it particularly attractive to DoD applications involving cryogenic focal-plane array (FPA) systems; namely, improved current gain at low temperature. Unlike a conventional Si bipolar transistor, whose gain quickly degrades upon cooling, the gain of the HBT can be made to increase upon cooling. The Hughes Aircraft Company (HAC) is currently a leading supplier of IR FPA systems to DoD. The sensing elements that are the "eyes" of these systems must be cryogenically cooled. In particular it is essential that read-out electronics interconnected to IR detector arrays operate at the detector operating temperatures (10 to 100K, depending upon application). It is desirable to locate signal conditioning and processing functions near the focal plane within the system dewar to minimize interconnections through the dewar vacuum seals. It will become essential to provide for this "on focal plane" signal processing capability as the size of arrays (especially in starring configurations) continues to increase. Currently most if not all such functions are provided by conventional Si electronics operating outside the dewar/optics subsystems and interconnected to the sensor by a large number of leads.

In addition to operating with high gains, low noise and more suitable power levels, it is also possible to simultaneously take advantage of the higher speeds already demonstrated for Si/SiGe HBTs to enhance the performance IR sensing systems.

1.3 PROGRAM APPROACH

$Si/Si_{1-x}Ge_x$ heterostructure materials are still in their infancy. Therefore, at this stage, any device program must still include significant material development. Our approach has been first to develop materials and then devices. Under this program, molecular beam epitaxy (MBE) is the growth technique used to form the Si and $Si_{1-x}Ge_x$ materials. Devices are fabricated with the use of standard Si processing techniques except those involving very high temperatures. The approach and techniques used to achieve our goals are summarized schematically in the diagram in Figure 1. The overall strategy is to produce Si and $Si_{1-x}Ge_x$ materials of acceptable crystalline quality, to establish dopant control of these materials, to fabricate and test basic HBT devices and to develop any special processing techniques which may be required, and finally, to modify the preceding processes as needed to result in optimized devices. We note that optimization is actually part of our long term strategy; in the present program, demonstration of HBT device behavior at room temperature and at cryogenic temperatures are our principal objectives.

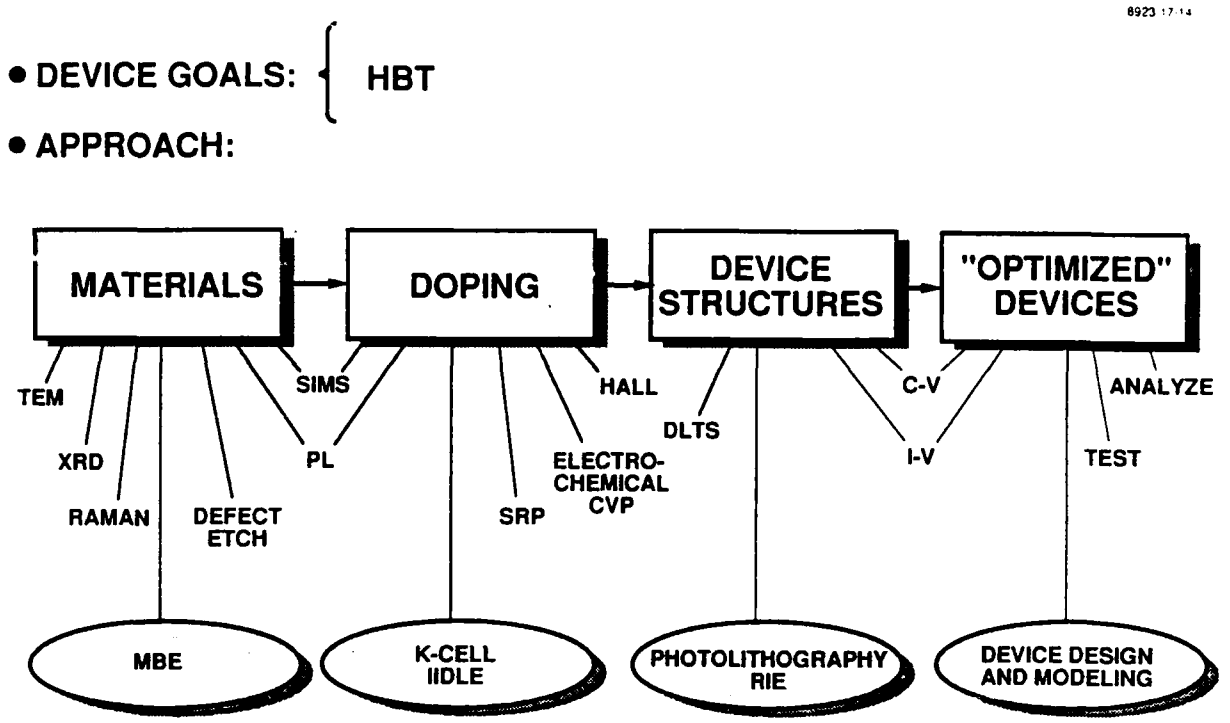

Figure 1. Program approach flowchart.

1.4 KEY RESULTS

We have established MBE growth and device fabrication processes which are suitable for fabrication of $Si/Si_{1-x}Ge_x/Si$ HBTs. We have measured room temperature current gains as high as 40 for our preliminary HBT devices. This gain represents an enhancement over current gains reported in the literature for homoepitaxial transistor structures of similar doping and layer thickness values. More importantly, we have measured current gain at cryogenic temperatures. In this report we shall present the first gain measurements performed at cryogenic temperatures down to 10 K for a $Si/Si_{1-x}Ge_x/Si$ HBT. Although the current gains of our HBTs are observed to decrease rather than increase with cooling, the rate of gain decrease is significantly less than that of an ordinary Si bipolar transistor. In particular, our HBTs at present retain approximately 16% of their room temperature gain values at 10K, an enormous relative improvement over that of homoepitaxial Si. Finally, we have designed our HBT mask set with sufficient flexibility in terms of device size, geometry, and possible device fabrication schemes to facilitate optimization in future efforts.

SECTION 2

MBE GROWTH OF HBT MATERIALS

2.1 MBE GROWTH

All $Si/Si_{1-x}Ge_x$ heterostructures studied under this program are produced by molecular beam epitaxy (MBE) in a Perkin-Elmer model 430-S Si MBE system. The Si MBE process involves codeposition of Si, Ge, and dopant fluxes onto a heated Si substrate under ultrahigh vacuum (UHV) conditions. Our MBE system contains dual 40-cc e-beam evaporators for co-deposition of Si and Ge, a substrate heater capable of heating a 3-in. diameter Si substrate wafer to temperatures up to 1250°C, and three Knudsen-type effusion sources for doping the films with Ga, B, or Sb. In situ characterization of surface crystalline quality of substrate and epitaxial films are accomplished through a reflection high energy electron diffraction (RHEED) apparatus. Stability in epitaxial growth conditions is achieved through feedback-stabilized control of Si and Ge deposition rates as well as substrate and effusion source temperatures during growth. In this way, epitaxial $Si_{1-x}Ge_x$ films of well controlled composition (x), layer thickness, and doping profile, can be produced.

MBE growth of all HBT structures is preceded by the following ex situ and in situ preparations. Heavily doped n-type Si (100) wafers (0.002 to 0.004 ohm-cm) are degreased in the organic solvents, tetrachloroethylene, acetone, and methanol, and rinsed in deionized water. Next, the wafers are subjected to an oxide removal etch consisting of 50% HF for approximately 1 to 2 min. The wafers are then cascade-rinsed in high-resistivity deionized water (18 Mohm-cm), dried, and immediately loaded into the MBE system load lock chamber. Under UHV ambient conditions, a single wafer is loaded into the growth chamber of the MBE system and heated to approximately 865°C in the presence of an 0.1 Å/s Si flux to desorb the native oxide and bury carbide domains. The success of this preparation is judged through the observation of a (2x1) Si surface reconstruction by means of RHEED.

After the above substrate preparation is performed, the epitaxial layers which constitute the HBT structure are deposited. The epitaxial structure is indicated in Figure 2. A thin (100 Å), nominally undoped buffer layer is first grown to achieve a good "template" for subsequent MBE layers. Next, we grow the collector layer, approximately 5000 Å thick, and doped n-type with Sb to approximately $1x10^{17}$ cm^{-3}, at a substrate temperature near 400°C. The substrate temperature is raised briefly to 850°C for 2 minutes to thermally desorb any Sb dopant from the surface, then brought down to 500°C. For the base, p-type, B-doped (nominally $6x10^{18}$ cm^{-3}) $Si_{1-x}Ge_x$ is deposited to a thickness of 500 or 1000 Å. Nominal compositions x were varied between 10 and 25%. The B flux is shut off for the last 10% of the base layer deposition in our

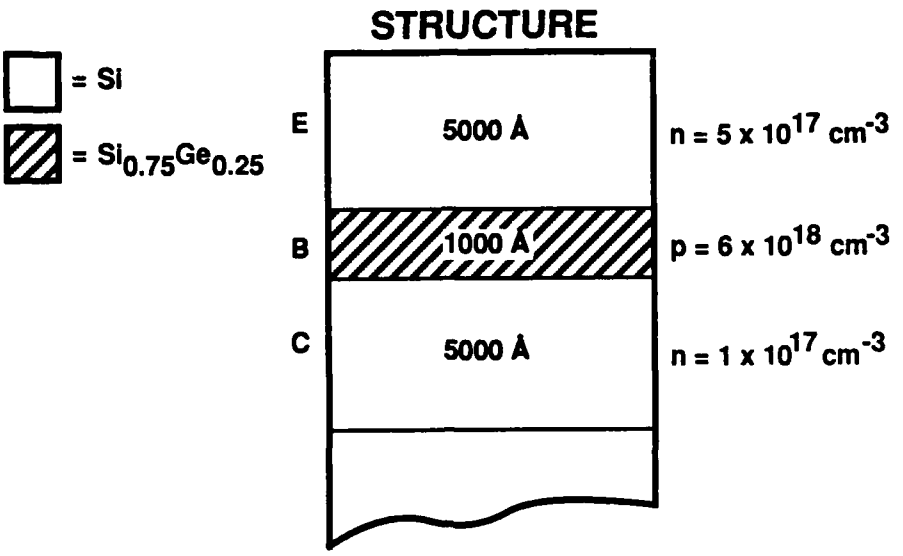

Figure 2. Epitaxial structure of the $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistor grown by MBE. For simplicity, buffer and top contact layers are omitted.

samples to ensure coincidence of the electrical and compositional junctions. Next, the substrate is cooled again to near 400°C and the 5000 Å emitter layer deposited to a nominal n-type doping of $5x10^{17}$ cm^{-3}. Just prior to emitter layer deposition, the Sb dopant flux is predeposited for 2 minutes to promote a sharper dopant profile increase at the beginning of the layer. (There is a tradeoff between Sb dopant profile abruptness and crystalline quality of the film as we discuss below.) Finally, a 1000 Å, very heavily Sb-doped (approximately 10^{19} cm^{-3}) n-type cap layer is deposited to facilitate electrical contact to the emitter. For simplicity, this cap layer as well as the initial 100 Å buffer layer are omitted from the drawing in Figure 2.

2.2 DOPING

During this program, to produce acceptable device layers it was necessary to solve some nontrivial phenomenological difficulties associated with the kinetics and thermodynamics of dopant incorporation during Si MBE growth. These difficulties arise due to surface segregation of the dopant during growth. Typically, the surface segregation phenomenon leads to very small incorporation coefficients and very long surface residence times of the dopant species, both of which are extremely sensitive to substrate temperature. Small incorporation coefficients limit the peak dopant concentration, and long residence times (the characteristic time over which the dopant concentration can change significantly during growth) ordinarily make sharp dopant profiles difficult to produce.

Most of the technologically important Si dopants which can be used in effusion sources in a manner consistent with a UHV deposition process exhibit this surface segregation behavior. The most frequently used dopants in Si MBE work at the time of this program are Ga (p-type) and Sb (n-type). Our initial $Si_{1-x}Ge_x$ layers were doped with Ga. However, we soon found this to be completely unsatisfactory. We found it essentially impossible to simultaneously achieve a high p-type Ga dopant concentration (at the levels needed in our HBT base layers) and dislocation-free, coherently strained growth of our $Si_{1-x}Ge_x$ layers although each was achieved separately. This problem was resolved through the use of elemental B as our p-type dopant. Elemental B, unlike almost all other Si dopants, does not undergo the aforementioned surface segregation behavior, and so avoids profile-smearing and peak-concentration problems described above. In order to make use of elemental B as dopant, it was necessary to acquire a special effusion source capable of significantly higher temperature operation. However, once acquired, we were able to produce B dopant profiles of excellent profile sharpness and very high peak dopant level, as shown in Figure 3.

The situation for n-type doping was more difficult, but was eventually solved through modifying and carefully controlling substrate temperature during deposition of n-type layers. The nature of the problem is illustrated in Figures 4(a) and 4(b). This figure shows the effect of a slight change in substrate temperature on crystalline quality. High resolution x-ray diffraction scans for the HBT structure indicated earlier in Figure 1 are shown here. The upper scan, corresponding to a sample with Sb-doped layers grown at a substrate temperature of 370°C (sample HA90.021), contains very broad peaks from the Si and $Si_{1-x}Ge_x$ epilayers due to a high dislocation density in the layers. The lower scan corresponds to a similar HBT with Sb-doped layers grown at 425°C (sample HA90.023). Note that there is a dramatic improvement in crystalline quality as evidenced by the considerably sharper x-ray peaks and the observation of several orders of Pendelossung fringes due to the finite thickness and extreme abruptness of the $Si_{1-x}Ge_x$ layer boundaries.

Figure 5 shows the dopant profile for the same two samples as determined through electrochemical capacitance-voltage profiling (ECVP) analysis. The principal difference is the sharpness of the profile corresponding to the Sb-doped layers. Dopant segregation is a thermally activated process. As the substrate temperature is lowered, the segregation kinetics become frozen out and the profile sharpens. Since, unfortunately, Si and Ge atom mobility on the growth surface is also reduced at lower substrate temperatures, there is a practical tradeoff between Sb dopant profile sharpness and crystalline quality as seen by comparing Figures 4 and 5. For the present work, crystalline quality is the more stringent requirement. For our preliminary work, it is sufficient to have the collector and emitter doping levels of the right approximate

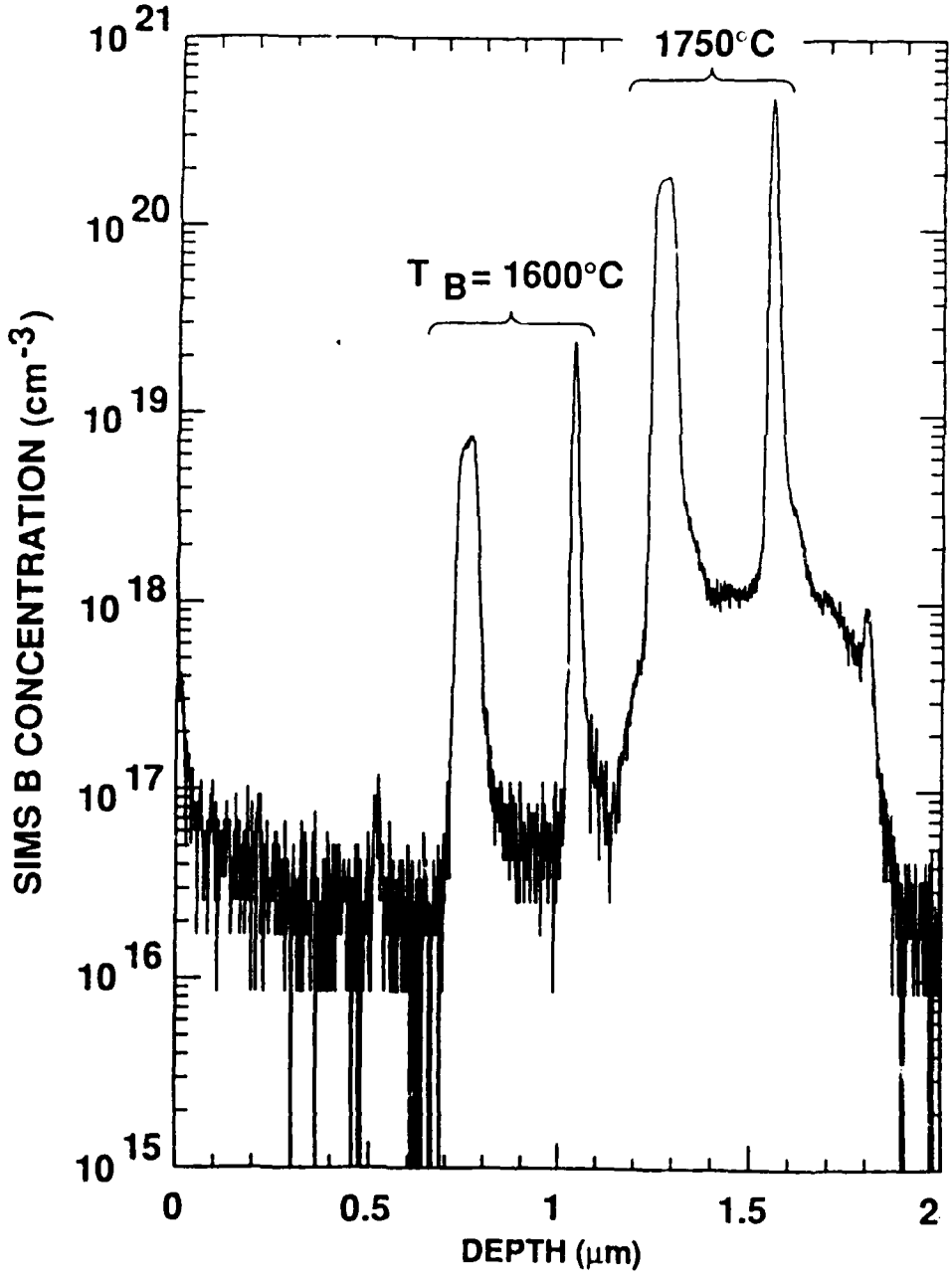

Figure 3. B delta-doping profile, demonstrating profile sharpness obtainable with MBE.

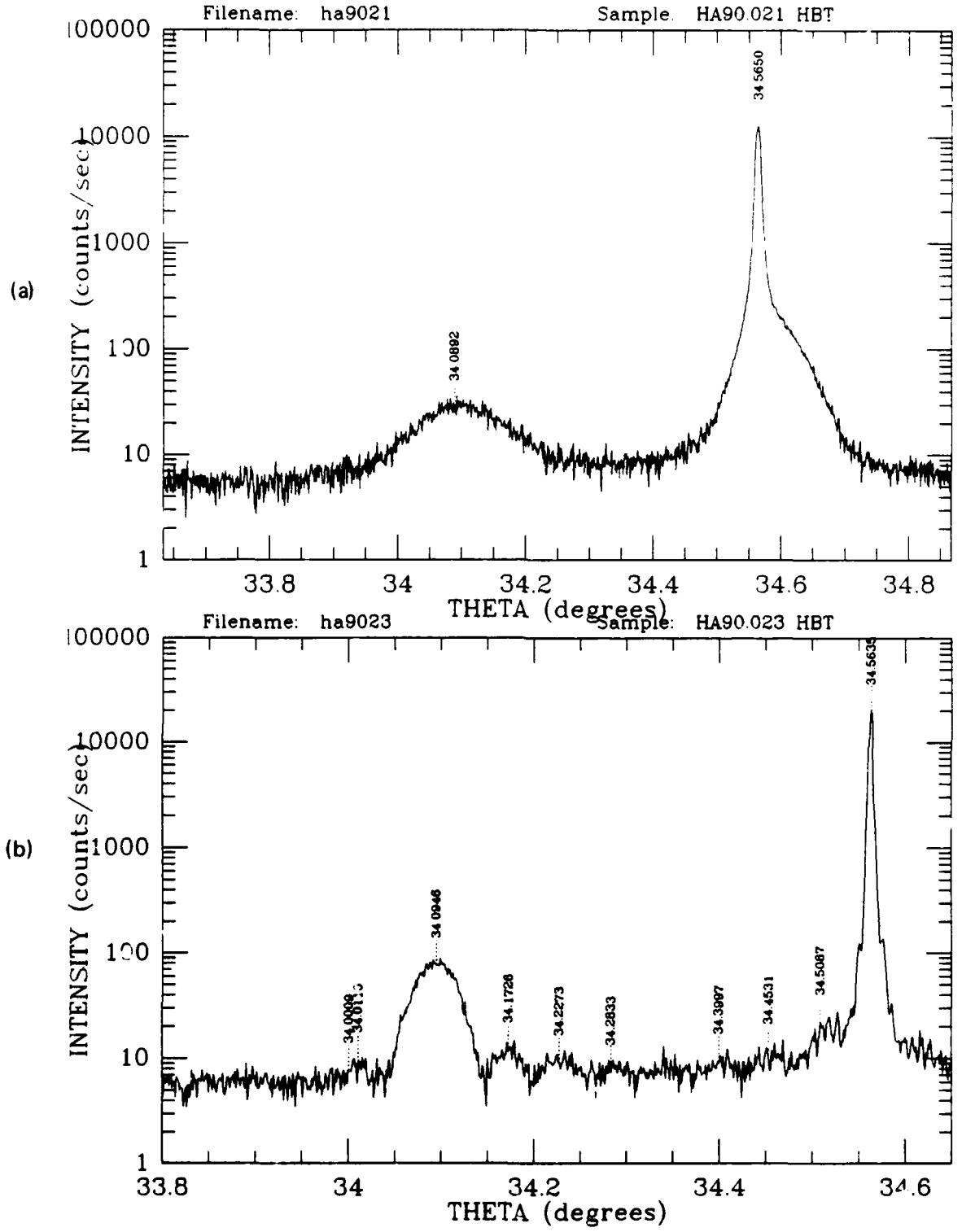

Figure 4. High resolution x-ray diffraction of samples (a) HA90.021 and (b) 0.023. HA90.021 is of poor crystalline quality while HA90.023 is perfectly coherently strained.

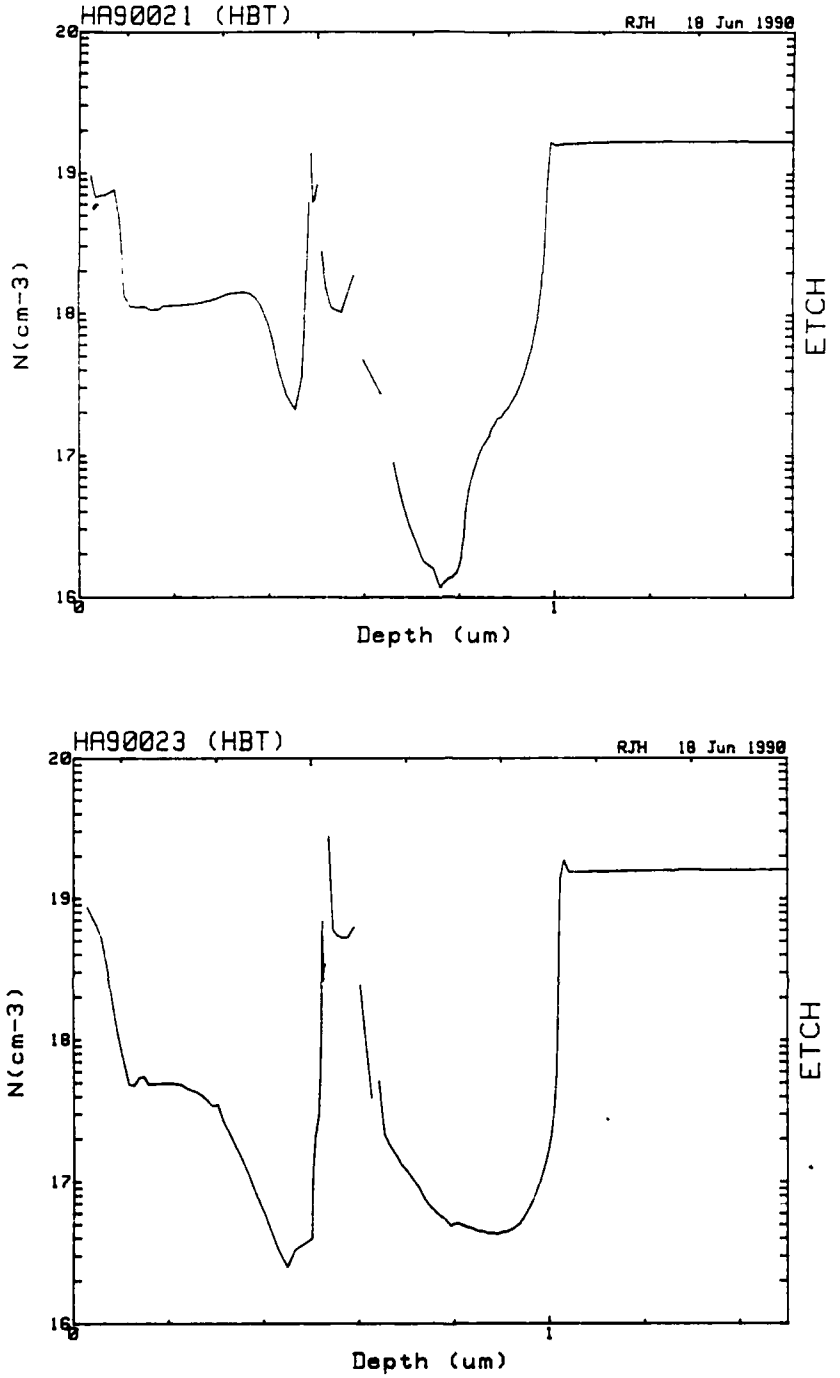

Figure 5. Dopant profile determined by electrochemical capacitance-voltage profile (ECVP) analysis. Dopant profiles for samples HA90.021 and 0.023 are shown. The profile of the former are fairly abrupt while the profile of the latter is more smeared out.

concentration, but these profiles need not be perfectly rectangular to demonstrate reasonably good transistor action. Accordingly, we view our 425°C samples to represent the appropriate tradeoff. This view is validated through the successful realization of HBTs, the device characteristics of which will be described below.

SECTION 3

FABRICATION AND PROCESSING OF HBT DEVICES

In May, 1990, our primary focus concentrated on device fabrication development. In this effort we enlisted expert assistance from Hughes Technology Center (HTC) in Carlsbad to develop device fabrication processes. Device design, process development and device fabrication were the emphasis of our work.

3.1 MASK SET

To create HBTs requires design and layout of a mask set containing the transistors desired, and in this case individual isolated transistors. In a cooperative effort between HRL and HTC, a mask set was laid out containing a variety of device geometries and sizes specifically for fabrication of the $Si/Si_{1-x}Ge_x/Si$ HBTs at HRL. The mask set used in this program was paid for with Hughes internal funds.

The mask set was designed with specific goals in mind. The first goal was to quickly fabricate discrete HBT devices to characterize the material and device properties. Second was to provide more than one type of device geometry for testing and evaluation to differentiate device design considerations from our testing and evaluations. Third was to provide more than one type of device processing technique to allow for comparisons with different process techniques. Various in-process test monitors were added to the mask set to allow for a verification of etching and lift-off steps of the process.

The HBT is a three terminal device, where the emitter and base contacts were made from the topside and the collector contact was made from the backside, through the substrate. In addition, two devices per mask field were added with topside collector contacts. These devices have the advantage of a lower resistive path from base to collector contact, however, they require an additional mask step to fabricate over the standard backside contact device.

A photo of the actual HBT devices fabricated with our mask set is shown in Figure 6. Device geometries were varied in shape and area/perimeter ratio, as well as having either topside or backside collector contacts. Device sizes varied with all combinations of emitter width (5 to 125 microns), base width (5 to 125 μm) and base to emitter spacing (2 to 7 μm). The mask set also accommodates two possible processing techniques, "implanted" devices and "mesa" structure devices. These two possible device structures are shown in Figure 7.

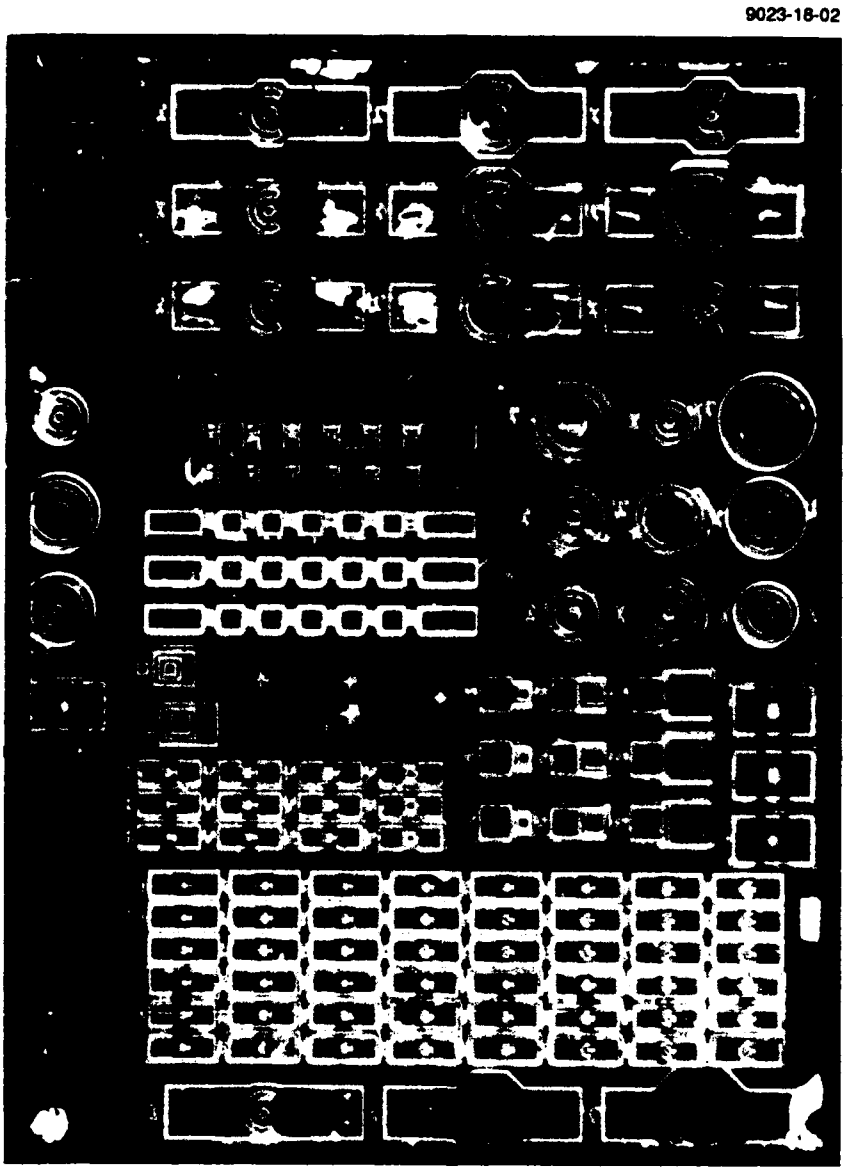

Figure 6. Photograph of the HBT mask set used in this work.

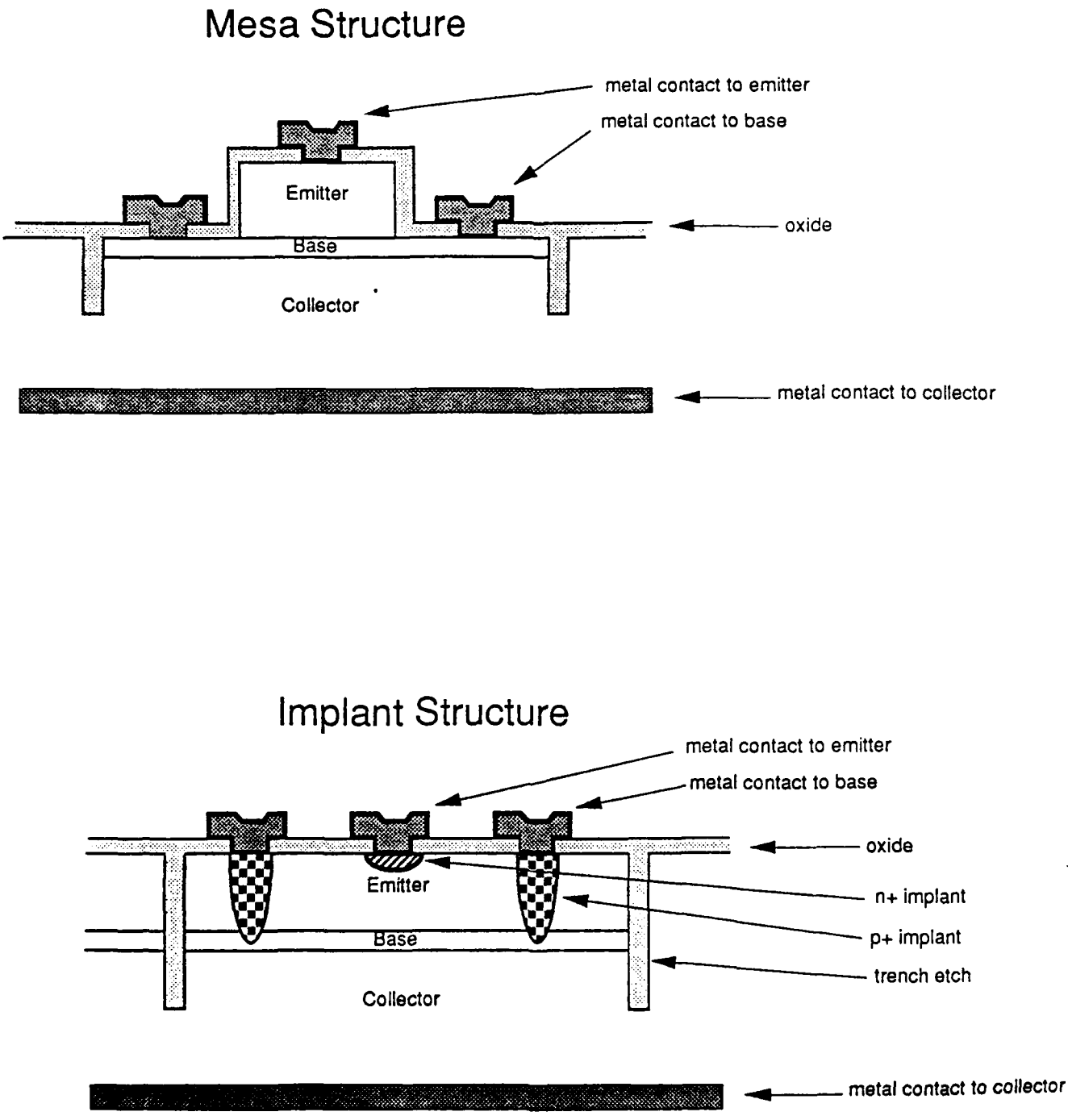

Figure 7. Schematic of "mesa" and "implant" device configurations.

3.2 PROCESSING

The implanted devices are made by implanting the base contacts through the emitter layer, requiring a double or triple boron implant to make p-type contact through the n-type emitter layer. The devices are isolated from each other with a $CF_4 + O_2$ Reactive Ion Etch (RIE) trench etch. For this particular device design, the trench is approximately 9000 Å deep, and cuts through both the emitter/base and base/collector junctions. These junctions are passivated with a deposited oxide, PECVD SiO_2 or Si_3N_4 deposited at 200°C. Openings are made in the oxide for metal contacts with the CT mask and a wet chemical etch. Al metal contacts are made with a lift-off process to the base, emitter and collector as shown in Figure 7.

The mesa structure is made by creating islands of emitter layer, and otherwise etching down to the base layer with a selective wet chemical etch. The wet etch is composed of KOH, water, $K_2Cr_2O_7$, and alcohol. Although this etch mixture is slow, with an etch rate of approximately 150 Å/min, it is very selective to the Ge content of the film and stops on the $Si_{1-x}Ge_x$ base layer. The devices are isolated with an RIE trench etch, ($CF_4 + O_2$ gas etch), that starts on the exposed base layer and etches through the base/collector junction, about 2500 Å deep. The surface of the device is passivated with deposited oxide, PECVD SiO_2 or Si_3N_4 deposited at 200°C. Contact openings are made in the oxide with a wet chemical etch. Al metal contacts are made to each layer with a lift-off process as shown in Figure 7.

Parametric test structures are also included in this mask set to do transmission line measurements, f_t measurements and for device process characterization. All total, there are 100 transistors per field of the mask set, with 465 fields covering a 3-inch wafer.

Process development for the $Si_{1-x}Ge_x$ devices was begun using the mesa device structure. Although we expect the implanted device design to produce a better quality device, there are many processing steps that we need to develop before we can produce the implanted device. The etchant disolves photoresist, thus an oxide mask was used to cover the mesa islands. An anisotropic RIE dry etch device isolation process was developed for these devices to isolate the base/collector junctions between devices. The anisotropic properties of this etch were needed to avoid undercutting the devices during the trench etch. Surface passivation is needed on devices of either design to reduce surface leakage currents which have been seen by many workers at exposed p-n junctions. We have deposited low temperature PECVD SiO_2 and Si_3N_4 dielectrics and found them not to alter the strained-layer properties of the $Si_{1-x}Ge_x$-base HBT structures. A metal lift-off process was used to make contact to the devices using aluminum as the contact metal, followed by a low temperature RTA anneal.

For this program, devices were made on six different material samples having actual base layer Ge content from 12 to 24% and base layer thicknesses from 460 to 1000 Å. Only the backside collector contact devices have been made thus far to reduce the number of mask steps needed and speed up processing time. High resolution x-ray measurements made before and after processing verify no change in sample quality from processing.

3.3 ELECTRICAL CHARACTERIZATION

The devices were tested via room temperature probing, and then packaged and wire bonded for cold temperature testing. The tests looked at both the emitter/base junction and the base/collector junction diodes as well as the transistor characteristics including gain, Gummel plots, and transistor and diode characteristics varying with temperature. The device measurement results are described in the next section.

SECTION 4

HBT RESULTS

The first devices tested were all large area devices, having some series resistance in each of the diode junctions. In the future we wish to study the smaller-area devices. Series resistance effects in smaller devices should be relatively less important, and material defects statistically less likely to affect the smaller devices. Also the ability to reach higher current densities experimentally should lead, to higher gains in the smaller devices.

Excellent devices were found even at the room temperature wafer probing level on most of the MBE samples. Gains as high as 40 have been achieved at room temperature via probe testing, with an average gain of 10 seen across the samples. Only one sample had gains of less than 5, and this sample was later shown via SIMS measurements to have a higher level of impurities than normal. The emitter/base and base/collector junctions were shown to have a very sharp, reverse bias breakdown at nominally -10V which is excellent for a test device of this design. The forward bias turn-on voltages are characteristic of a large-area device having non-negligible series resistance.

We found these large area HBT devices to operate at 10K (our lowest testing temperature), with gain. Although thus far we have found the gain to decrease with temperature rather than increase, as expected, we are encouraged with the operating performance of these devices at cryogenic temperatures since material properties were not optimized for very low cryogenic temperature operation in the initial studies.

4.1 SAMPLES GROWN/DEVICES PROCESSED

The set of $Si/Si_{1-x}Ge_x/Si$ HBT samples grown in this study is summarized in Table 1. These samples all consist (from the top down) of a 1000 Å Si contact layer, a 5000 Å emitter layer, a 500 Å or 1000 Å $Si_{1-x}Ge_x$ base layer, a 5000 Å Si collector layer, and a thin, undoped, 100 Å buffer layer, all grown onto degenerate n-(100) Si substrates. The nominal dopings are $5x10^{17}$, $6x10^{18}$, and $1x10^{17}$ cm^{-3} in the emitter, base, and collector layers, respectively, with the substrate and top contact layers doped in the 10^{19} cm^{-3} range. The principal parametric variation is in base Ge content x. In addition, for some samples, base thickness is varied, other factors being held constant, and for other samples, there was a deliberate variation in doping levels. The epitaxial layers in these samples have been characterized for crystalline quality, base layer thickness, and Ge content by means of high resolution x-ray diffraction, and for carrier profile through ECVP analysis. In some cases, other characterizations such as Rutherford backscattering spectroscopy (RBS) or secondary ion mass spectroscopy (SIMS) have been

TABLE 1. SUMMARY OF MBE-GROWN HBT STRUCTURES

Sample	Strain	Base x (%)	Base thk (A°)	N_E (10^{17} cm^{-3})	N_B (10^{18} cm^{-3})	N_C (10^{17} cm^{-3})
PE89.074	----	0	5000	1	5	1
PE89.078	COH	12	1000	1	5	1
PE89.079	COH	12	500	1	5	1
PE89.080	RLX	>20*	1000	1	5	1
PE89.081	RLX	>20*	500	1	5	1
HA90.012	COH	12	1000	5	6	1
HA90.013	~COH	9	1000	5	6	1
HA90.020	~COH	22	1000	5	6	1
HA90.021	~COH	16	1000	5	6	1
HA90.022	COH	17	1000	5	6	1
HA90.023	COH	16	1000	5	6	1
HA90.024	COH	24	1000	5	6	1
HA90.025	COH	18	500	5	6	1
HA90.026	COH	21	500	5	6	1
HA90.027	COH	24	500	10	6	1

*Composition could not be determined accurately due to strain relaxation.

performed to provide corroborative or additional information about material quality, dopant profile, and impurity identification. The crystalline quality is indicated qualitatively in Table 1 under the heading, "Strain". In this category, "COH" denotes a high quality coherently strained film, "~COH" denotes coherently strained but with a high density of threading dislocations, and "RLX" denotes a relaxed, low quality structure.

4.2 ROOM-TEMPERATURE DEVICE CHARACTERISTICS

At room temperature, we examined common-emitter transistor characteristics, and also looked at emitter-base and collector-base diode characteristics. Figure 8 shows three sets of characteristics for a device on piece 24A: common-emitter characteristics, emitter-base junction

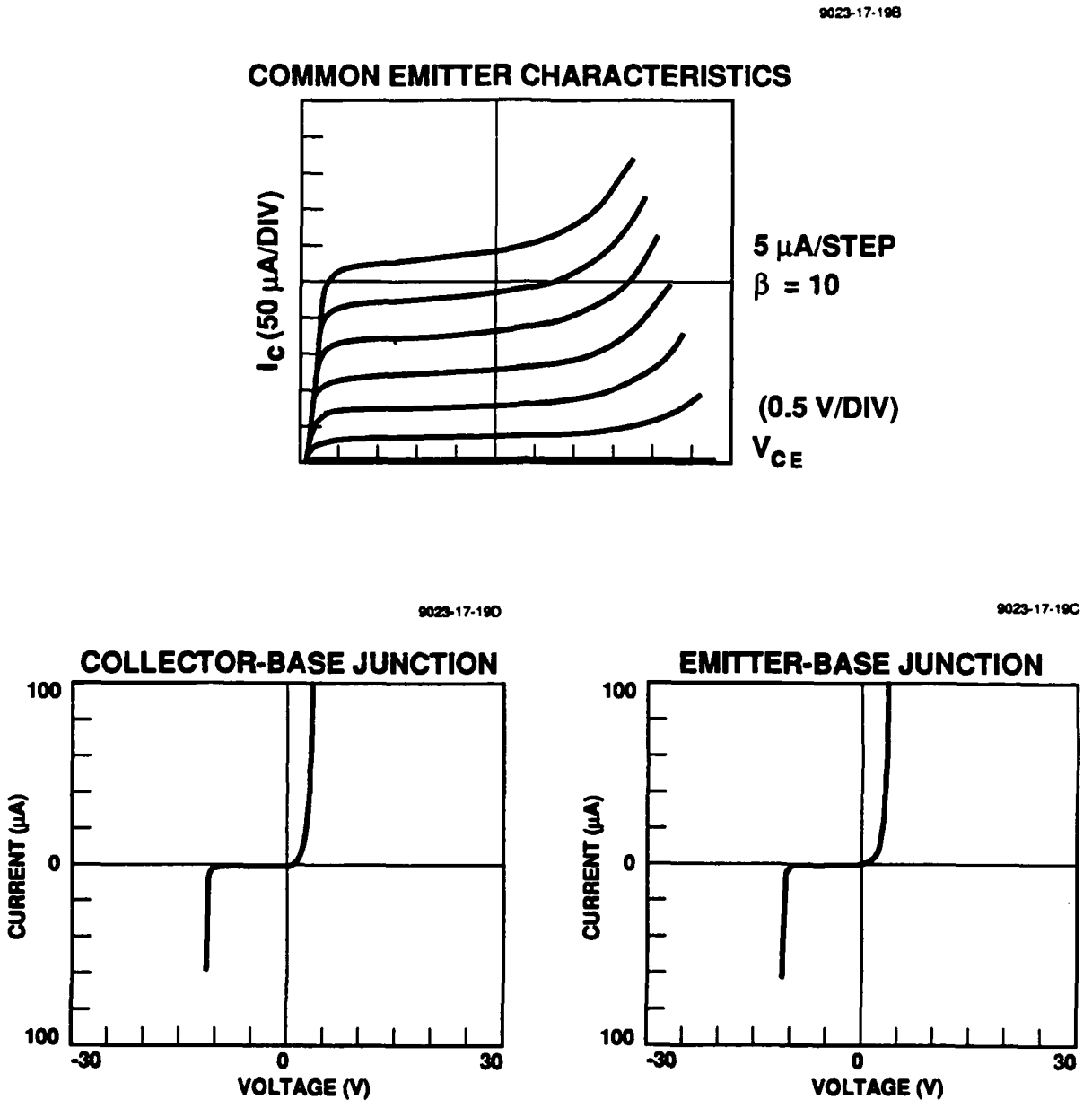

Figure 8. Electrical characteristics of HBT device #24A3. Shown are the common-emitter characteristics, emitter-base diode characteristics, and collector-base diode characteristics, at T=300 K.

diode characteristics, and diode characteristics for the collector-base junction. The common-emitter characteristics show qualitatively expected bipolar transistor behavior, and yield a current gain of 10 for this particular device. For the same device, both the emitter-base and collector-base junctions show very high-quality diode behavior, with large rectification ratios, very abrupt or "hard" reverse breakdown characteristics at voltages consistent with the levels of doping in these structures, and in forward bias, reasonably good ideality factors, particularly for the collector-base diodes. Our diodes show series-resistance-limited behavior for sufficiently large forward bias values. This is due in part to our emphasis on fabricating the large-area devices initially. (Fabrication of the smaller devices on our mask sets presented no fundamental difficulties but did require more precision and care to fabricate successfully than we deemed was warranted in these initial attempts.)

The room temperature characteristics of our HBT devices are summarized in Table 2. Among the MBE samples looked at so far, the one yielding the best results on a consistent basis is sample HA90.024. From Table 2, we see that typical current gain values for devices on piece 24A range from 10 to 22. (In Table 2, processed specimens are labeled according to the suffix of the MBE sample name corresponding to the MBE wafer from which the specimen was taken; A, B, C, etc., refers to multiple, separately processed pieces of the indicated MBE sample.) Additionally, the diode characteristics associated with these devices consistently yield hard reverse breakdown characteristics with V_{rev} = -10 to -13 V.

Gummel plots were also made for selected devices. Figure 9 shows the Gummel plot of HBT device #3 on piece 24A, denoted as #24A3 in the figure. In the Gummel plot, we see that, for this device, for V_{BE} greater than approximately 0.6 V, the collector current parallels the base current with a current gain of about 10. For smaller values of V_{BE}, the current gain decreases. The effect of series resistance is apparent as there is no clearly linear region of either I_C or I_B versus V_{BE} in the figure.

Examination of Table 2 shows that, in terms of typical device behavior, pieces from sample HA90.024 yield the highest gains and the hardest reverse breakdown characteristics. In terms of MBE material quality, HA90.024 is among the best of our samples thus far. However, some exceptions to these general trends are occasionally observed. For example, the HBT which exhibits the highest gain at room temperature (gain = 40) was a single device from piece 21. The common-emitter characteristics of this device are shown in Figure 10. On comparing Figures 10 and 8, we see that, despite the greater gain of the device shown in Figure 10, the device appears much more saturation-current limited, and the ac gain a relatively much stronger function of I_C and V_{CE}. Not shown in Figure 10 are the diode characteristics, which are comparatively poor, exhibiting soft reverse breakdown characteristics. The increased leakage current in reverse bias is expected since the $Si/Si_{1-x}Ge_x$ heterojunction in this device is known from our x-ray

TABLE 2. HRL Si/SiGe HBT SUMMARY

LAYER	X-RAY	% Ge	BASE THICKNESS	BREAKDOWN VOLTAGE	VBR COMMENTS	TYPICAL GAIN	
24A	Excellent	24	920A	10-13	hard	10-22	
27				6-8	hard	~8	
21	Poor	17	1000	5-9	soft	~5	
23	Excellent	16	1000	6-8	med	~8	
12	Excellent	12	1000	2-5	soft	1	
26	Excellent	21	460A	8-10	hard	10	
24B	Excellent	24	920A	8-10	hard		
24C	Excellent	24	920A	7-10	med		edge piece

*NOTE: Best gain (40) was obtained at 300K on one device from HA90.021.

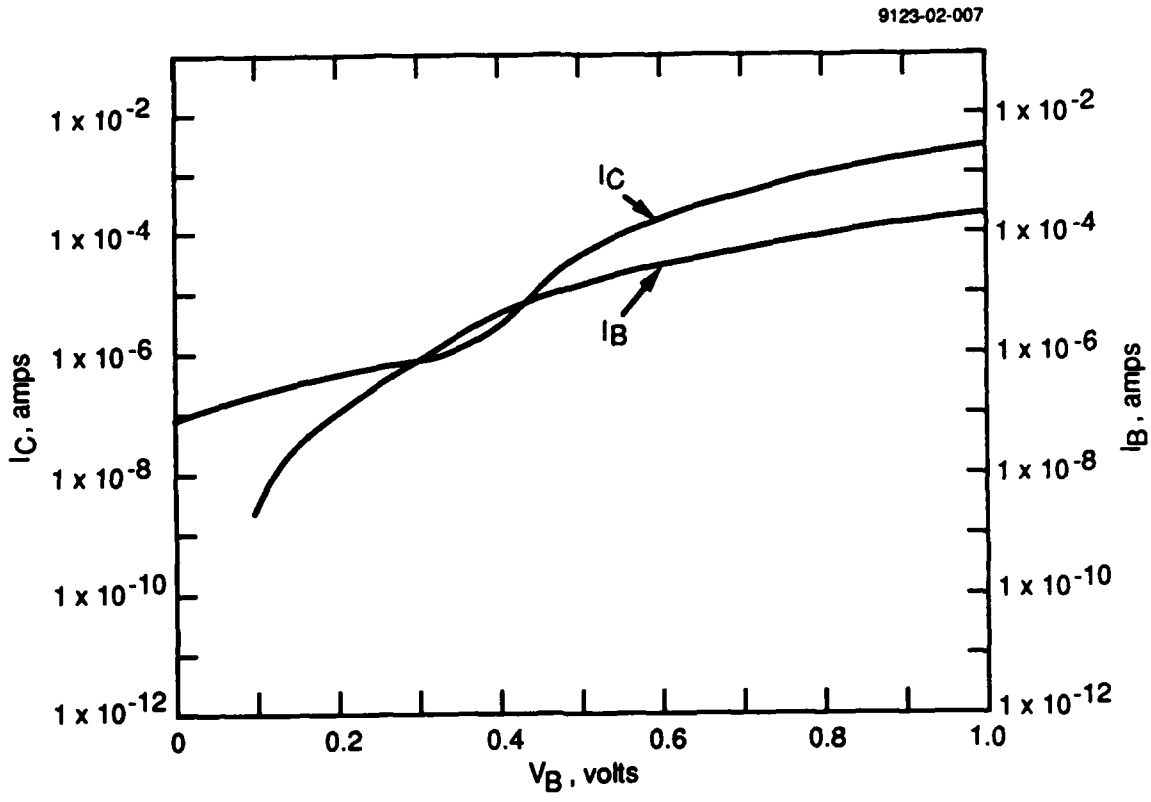

Figure 9. Gummel plot for HBT device #24A3.

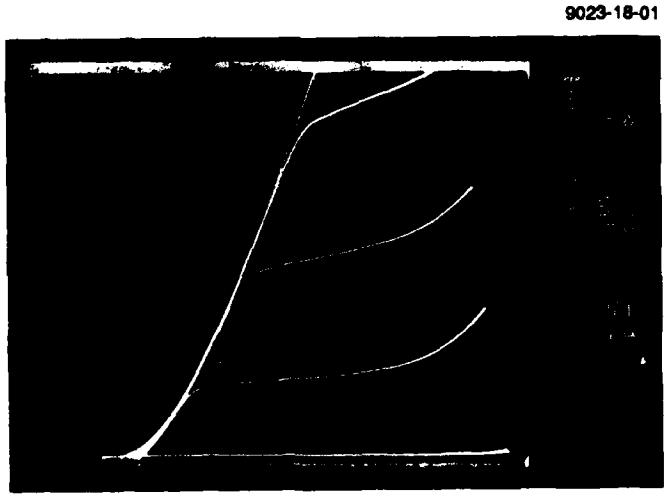

Figure 10. Common-emitter characteristics for device showing the highest room temperature current gain (from piece #21). The gain is approximately 40.

measurements to contain a much higher dislocation density and the overall material quality is poorer than for sample 24A. More significantly, the device shown in Figure 10 degraded irreversibly when low-temperature testing was attempted. It is possible that stresses induced by thermal expansion coefficient mismatch resulted in plastic deformation of the sample as it was cooled. This sample may have been more susceptible to such deformation than the higher quality samples since piece 21 already contained a large number of threading dislocations.

Figure 11 shows a comparison of common-emitter and common-collector characteristics for device #1 on piece 24A. In the upper set of curves, the HBT is connected electrically in the normal fashion with the emitter grounded. In the lower curves, the emitter and collector connections are exchanged. We see that there is a significant difference in current gain between the normal and reversed configurations: approximately 20 for the normal, and 0.07 for the reversed hookup. For the same device, the emitter-base and collector-base diode forward characteristics are shown in Figure 12. Also shown in Figure 12 is a line of slope 59.5 mV/decade, corresponding to a diode ideality factor of unity at 300K. The figure clearly shows that the collector-base junction of this device is of extremely high quality whereas the emitter-base junction exhibits leakage-dominated behavior (ideality factor approximately 2) below approximately 0.4 V. The greater leakage of the emitter-base junction is most likely a consequence of surface recombination. In the mesa device structure of Figure 7, there is necessarily free base surface area which must be adequately passivated in order to minimize surface recombination. In contrast, the base-collector junction is buried within the epitaxial structure, and only the side walls of the trench etch (which are also passivated) can potentially contribute area for surface recombination. Since the latter area is much smaller in comparison to the junction area than is the case for the emitter junction, a relatively smaller surface recombination current in comparison to the bulk diffusion current will flow. This observation is significant as base surface recombination current is a gain-reduction mechanism. It is expected that our implanted device structure (shown in Figure 7) will permit higher gain values in the future.

The diode characteristics of Figure 12 would suggest that significantly less recombination is occurring in the base-collector than in the base-emitter junction. This result is somewhat surprising in view of the significantly better gain of this device when in the normal rather than reversed configuration (Figure 11). One would have expected the more leaky emitter-base junction to lead to lower gain in the forward configuration, all other things being equal. Now, it is true that the intended emitter layer is more heavily doped by about a factor of five than is the collector layer. Theoretically, the gain is directly proportional to the "emitter"/base doping ratio, leading to an expected gain ratio of about 5 between the normal and reversed configurations of Figure 11, in the absence of any other differences between forward and reverse configurations.[2]

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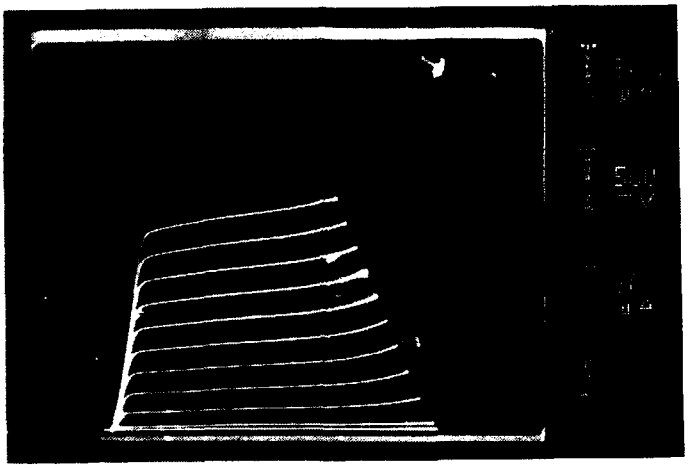
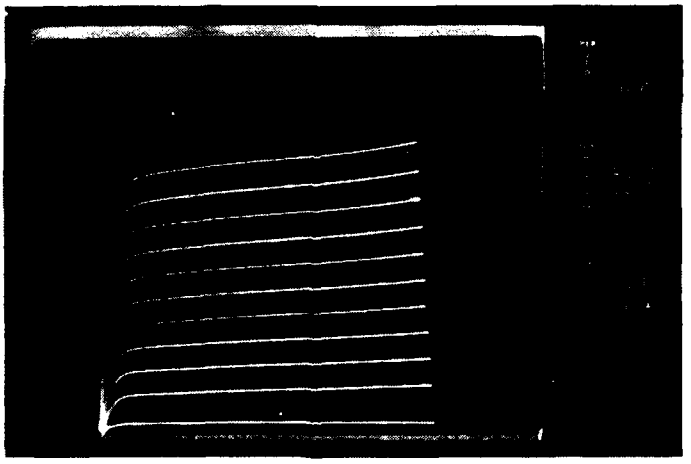
(a)



NORMAL

(b)



REVERSED

Figure 11. Common-emitter characteristics for device #24A1 with device connected normally; with emitter and collector leads interchanged.

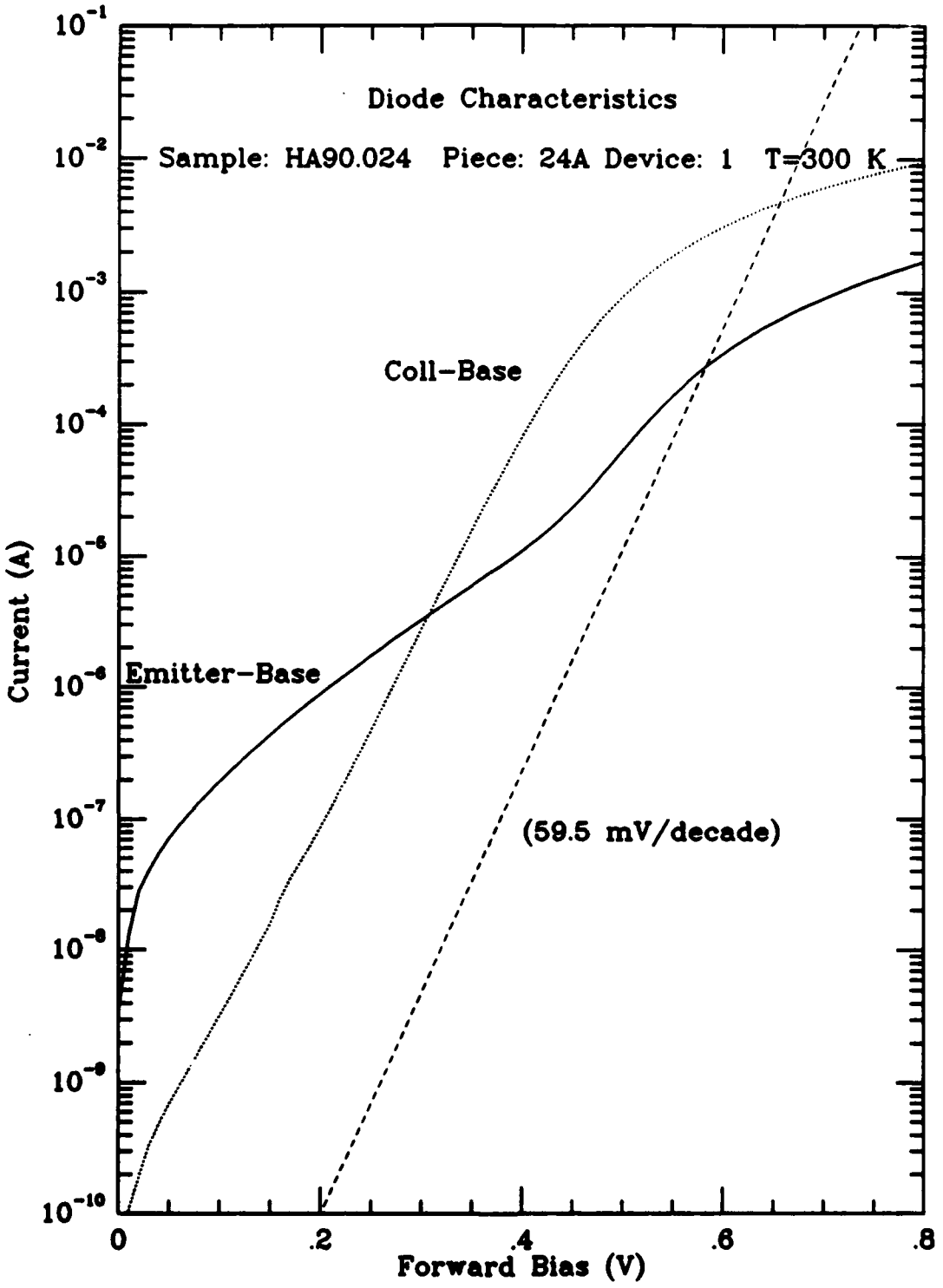


Figure 12. Emitter-base and collector-base diode characteristics for device #24A1.

However, the actual gain ratio is dramatically different (20/0.07 = 280). It is unlikely that the crystalline quality of the emitter-base and collector-base interfaces is significantly different. Also, SIMS analysis shows that the actual n-type dopant profiles are not perfectly rectangular (this was also seen earlier in Figure 5), but the profiles are flat enough on the scale of the Debye length of the n-type layers so that effectively they should be sufficiently flat. Hence, the origin of the dramatically different gains for forward and reverse configurations of Figure 11 is not understood at this time.

However, it is clear that gain-limiting mechanisms are present in our HBT devices. Comparison of our gains (~5 to 40) with gains of similar HBT structures reported in the literature[2-5] (~200 to 1000) also demonstrate this. Hence, the heterojunction-induced gain enhancement is being partially offset by non-idealities in our samples. On the other hand, our results present clear evidence of enhanced gain over homojunction devices. Our HBT devices exhibit gain despite the fact that the emitter is doped less than a tenth as heavily as the base. A homojunction transistor of similar layer thicknesses to our HBT devices and with identical emitter and collector doping levels (near 10^{18} cm^{-3}) is expected to show a gain[2] of approximately 2. Scaling this result by the emitter and base dopings used in this work corresponds to a gain of approximately 0.2 for the homoepitaxial transistor, in comparison to our observed HBT gains of ~5 to 40. In the next section, we shall examine the effect of temperature on our HBT device characteristics, and we shall see that the presence of the heterojunction gives rise to dramatic improvement in gain at low temperature, but that the gain-limiting mechanisms rather than the heterojunction itself are determining the actual temperature dependence of gain in our devices.

4.3 TEMPERATURE-DEPENDENT CHARACTERISTICS

We have measured the temperature dependence of HBT device characteristics for pieces 24A and 21. As noted above, sample(s) 24 and 21 are considered "good" and "poor" specimens, respectively, with respect to epitaxial quality. The common-emitter characteristics at several temperatures between 300 and 10K are shown for device #24A1 in Figure 13. The most important feature to note in this figure is that transistor behavior is retained all the way down to 10K. This is a remarkable improvement over conventional Si bipolar transistors.

From the data shown in Figure 13, we can obtain the gain as a function of temperature. This is shown in Figure 14. There, we see that the gain at 80K is 7.5, or about 40% of the room temperature value (17.5 in this case), and even all the way down to 10K, the gain is 2.4, which is 14% of the value at 300K. This is the first time a $Si/Si_{1-x}Ge_x/Si$ HBT gain has been measured at such a low temperature.

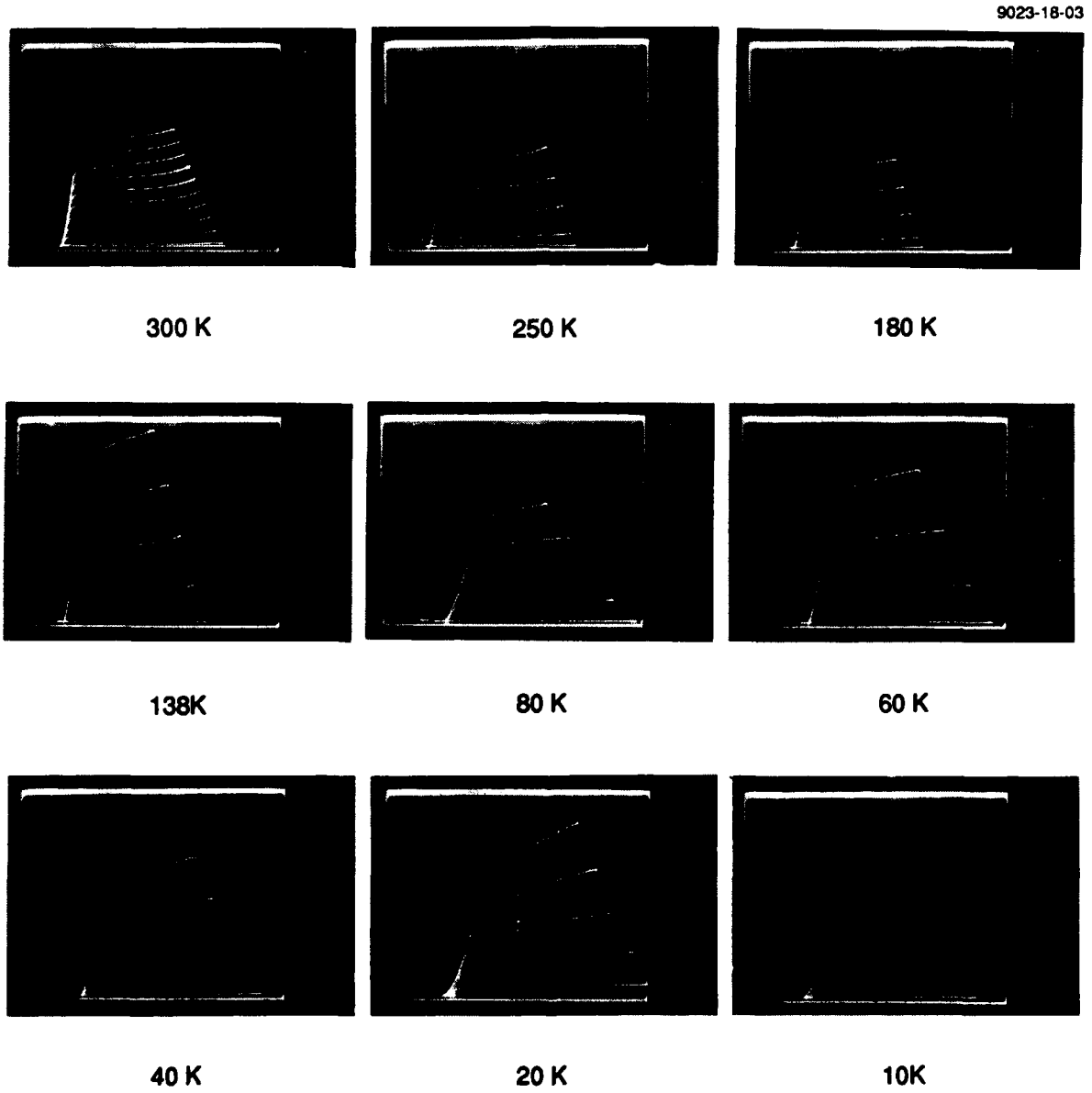


Figure 13. Common-emitter characteristics for device #24A1 at selected temperatures between 300 and 10K.

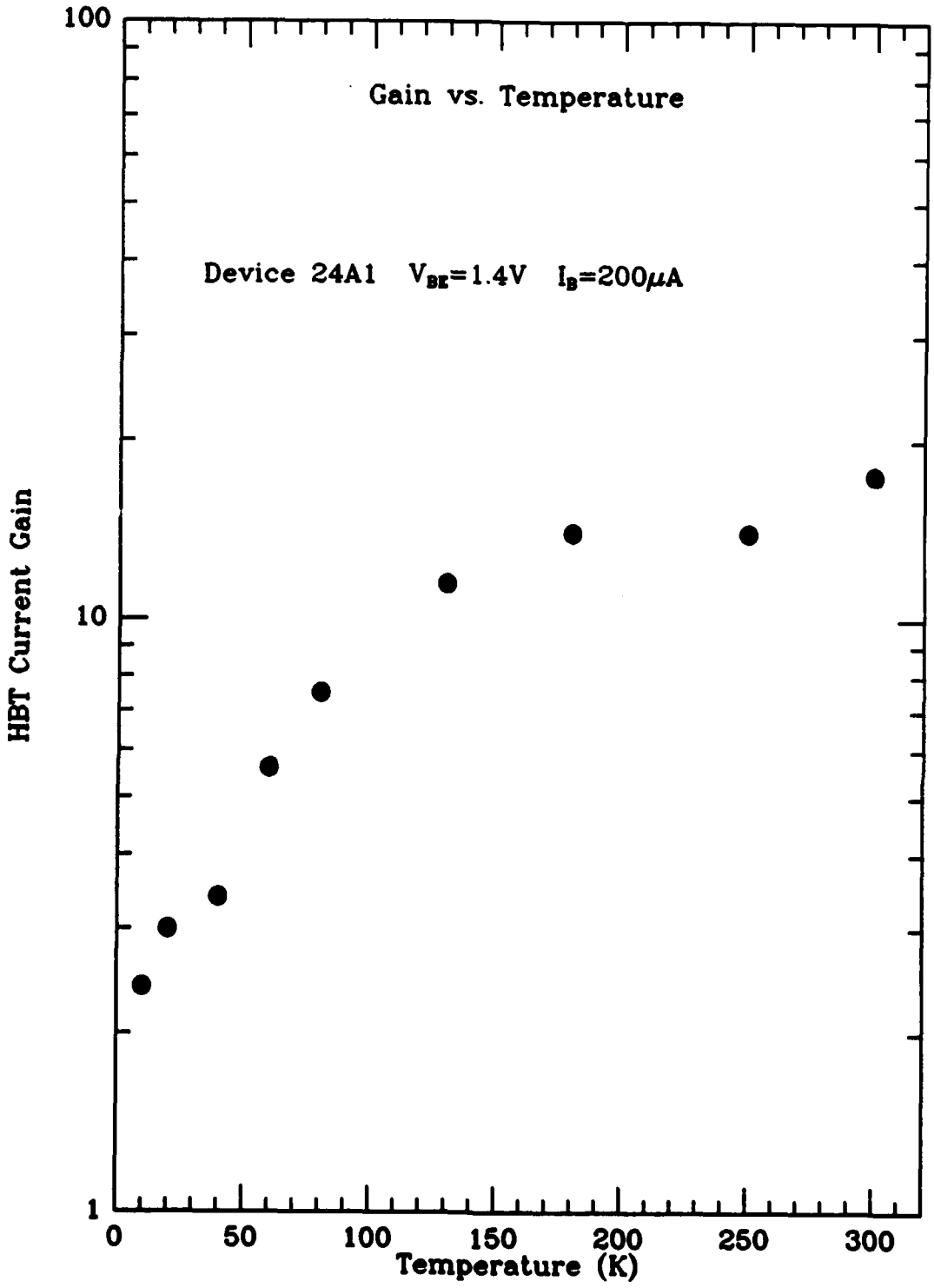


Figure 14. Current gain versus temperature for HBT device #24A1.

Theoretically, the gain is expected to increase with temperature for the n-p-n $Si/Si_{1-x}Ge_x/Si$ HBT, according to a Boltzmann factor whose activation energy is equal to the valence band offset (approximately 150 meV for our samples) between Si and $Si_{1-x}Ge_x$ when the latter is coherently strained to the former. To more quantitatively characterize the temperature dependence of gain, we have replotted the data of Figure 14 versus 1/T as shown in Figure 15. There, the data clearly exhibit two distinct regimes of thermally activated behavior. The higher temperature regime is associated with an activation energy of 7 meV, and the lower with an energy of 0.4 meV. The transition between the two regimes occurs at a temperature near 45K. It is unclear from the present measurements precisely what physical phenomena are responsible for the observed temperature dependence. In ordinary Si, gain reduction occurs due to bandgap narrowing (due to the high emitter doping levels needed for large room temperature gains) with an activation energy near 50 or 60 meV typically, depending on emitter doping level.[6] This effect should not occur here, and indeed, in principle should be overcompensated for by the $Si/Si_{1-x}Ge_x$ valence band offset, leading to a gain enhancement with cooling. Carrier freezeout is another possible process which is thermally activated and which would affect the gain. As to the knee in the data in Figure 15, it is possible that this is associated with a transition in current conduction mechanism from normal drift and diffusion to impurity-band conduction. However, identification of the physical origins of the temperature dependence shown in Figure 15 will have to await further study.

A comparison of the temperature dependence of gain of our $Si/Si_{1-x}Ge_x/Si$ HBT with an all-Si transistor is shown in Figure 16. Figure 16(a) shows a comparison of absolute gains for our HBT and for a poly-Si emitter device which has been optimized for high gain at low temperature. (The latter device was produced at HTC under an internal research and development program.) Also indicated is the gain of an off-the-shelf discrete Si transistor measured at two temperatures, 300 and 77K. As the data shows, the absolute gain of the Si transistors is higher at room temperature, but as the devices are cooled, the falloff in gain is much more rapid for the Si transistors than for the HBT, and, at low temperatures, the absolute gain of the HBT is the highest. Perhaps a fairer comparison between transistors would be to compare their normalized gains (normalizing each transistor's gain to its room-temperature value). Such a comparison is shown in Figure 16(b). In this case, the HBT clearly has the superior low temperature behavior. Comparison of normalized rather than absolute gains is reasonable because, ideally, the temperature dependence of normalized gain should not depend on the absolute gain value at room temperature. Furthermore, as we mentioned earlier in the preceding section, the gain behavior in our HBT devices appears to be limited by as yet unidentified gain-reduction mechanisms. Hence, if these were not present, the absolute gain, even at room

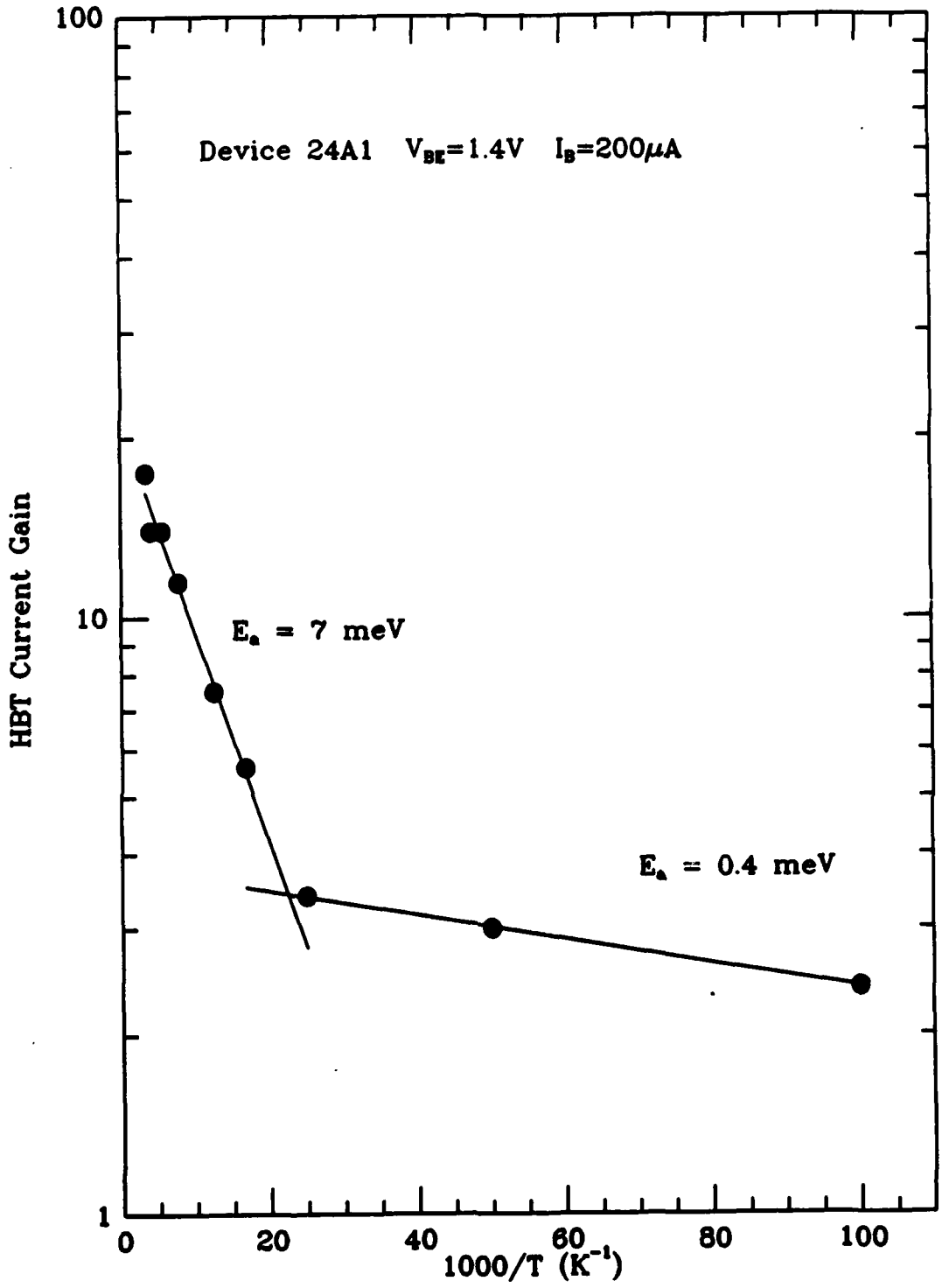


Figure 15. Gain data for HBT device #24A1 plotted for activation energy analysis. Two distinct regimes, having activation energies of 7 and 0.4 meV, and a crossover near 45°C, are seen.

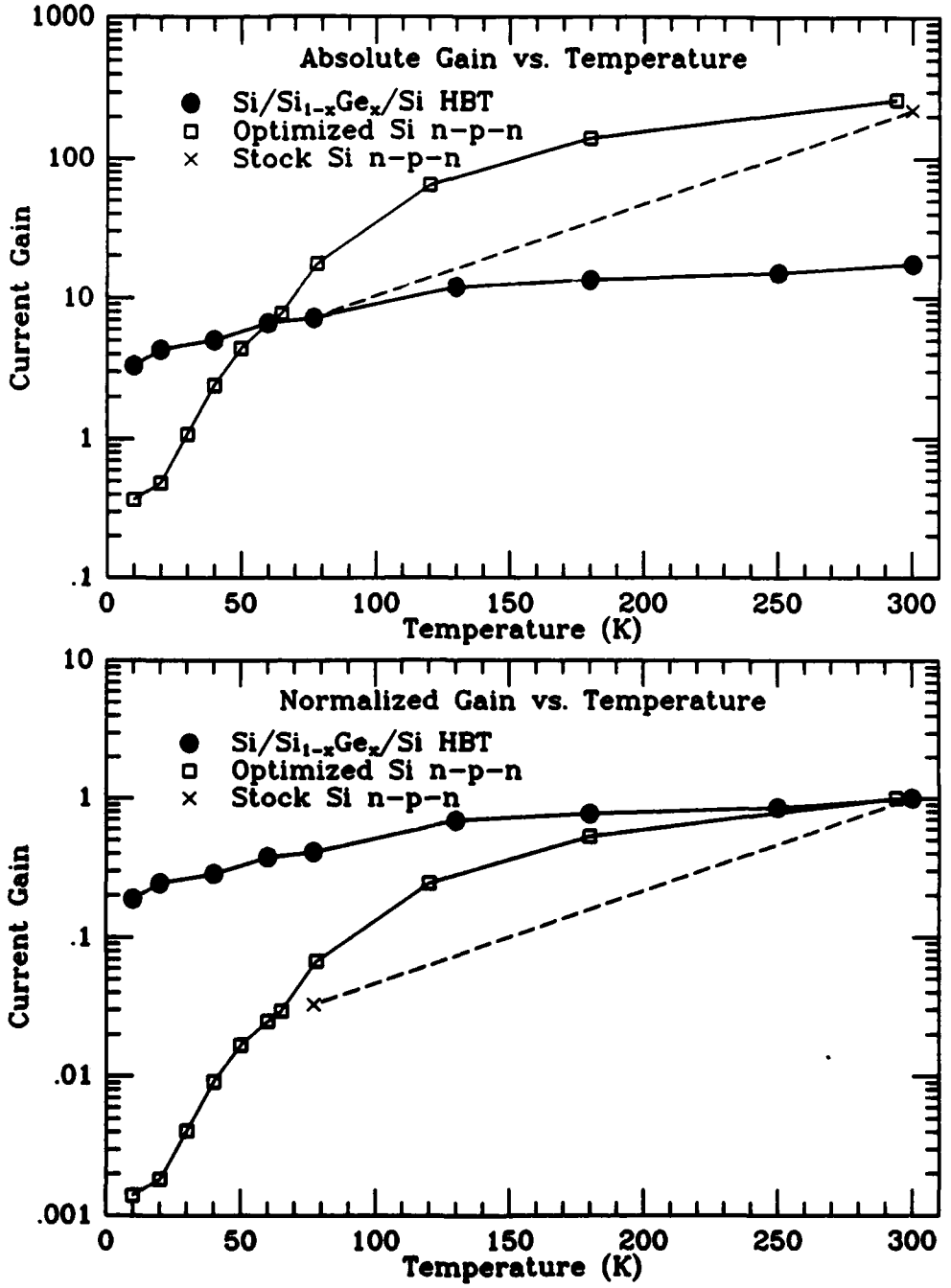


Figure 16. Comparison of HBT gain versus temperature performance to that of all-Si bipolar transistors. (a) Absolute gains. (b) Gains normalized to room temperature values.

section, the gain behavior in our HBT devices appears to be limited by as yet unidentified gain-reduction mechanisms. Hence, if these were not present, the absolute gain, even at room temperature, as well as the relative gain changes with temperature, should both be superior for the HBT in comparison to the all-Si transistors.

SECTION 5

SUMMARY

In summary, we have developed processes for the MBE growth and device fabrication of n-p-n $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors. We have characterized our devices electrically at room temperature and at cryogenic temperatures down to 10K. Our HBT devices exhibit transistor behavior with the best room temperature gains near 40, for a structure in which the emitter doping is $5x10^{17}$ cm^{-3} and the base is more heavily doped at $6x10^{18}$ cm^{-3}. The achievement of such a gain is direct evidence of the gain enhancement arising due to the $Si/Si_{1-x}Ge_x$ heterojunction. More importantly, we have made the first measurement of HBT gain at very low temperatures. Our HBTs exhibit only a modest gain reduction upon cooling. This gain reduction is drastically less than that of even optimized poly-emitter all-Si bipolar transistors. At present, the actual gain of our existing HBT devices appears to be limited, both at room temperature and at cryogenic temperature, by as yet unidentified physical processes. Despite these limitations, however, the low-temperature behavior displayed by our HBT devices appears encouraging, and the $Si/Si_{1-x}Ge_x/Si$ HBT appears particularly suited to DoD and other applications involving signal processing electronics in cryogenic focal plane array systems.

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